REMARKS

Prior to this Response, an Office Action was issued, mailed February 13, 2002.

In the Office Action, claims 5-7 and 9 were rejected.

In this Response, claims 5 and 7 have been amended.

The amendments to the claims constitute a bona fide attempt by the applicant to advance the prosecution of the application and obtain allowance, and are in no way meant to acquiesce to the substance of the Examiner's rejection. It is believed that the amendments to the claims place them in condition for allowance and/or in better form for consideration on appeal. These amendments were not made earlier because the amendments previously made were believed to place the application in condition for allowance.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Claims 5-7 and 9 are now pending in the present application. Reconsideration is requested. In addition to the referenced amendments, the Applicant makes the following remarks regarding individual issues:

The Applicant's time to respond.

The last Office Action was mailed on February 13, 2002. A two month period for responding to this Final Office Action expires on April 13, 2002.

Since the deadline falls on a Saturday, the deadline is extended to Monday, April 15, 2002 . (37 C.F.R. section 1.7.)

In determining whether this document is timely filed, the U.S.A. Patent Office is asked to note the Applicant's Certificate of Facsimile submission in conjunction with 37 C.F.R. section 1.8. That is notwithstanding when the present document is actually received by the U.S.A. Patent Office.

The Patentability Over Subramanian et al. (5,668,021):

Claims 5-7 and 9 are rejected under 35 U.S.C 103(a) as being unpatentable over Subramanian et al. (5,668,021) in view of Admitted Prior Art.

Applicant respectfully traverses this rejection.

Subramanian teaches forming a MOS device having a segmented channel region with a *buried* junction 24 (FIG. 7) in a central portion the channel (column 2, lines 45-47). Subramanian further teaches to form such MOS device with *non-uniform* channel doping (see, e.g., column 1, line 66 to column 2, line 2). In making the buried junction 24,

Subramanian teaches using an implant energy to establish a peak dopant concentration for th *buried junction below the surface* of the semiconductor substrate (column 3, lines 63-67).

Applicant submits that Subramanian does not disclose a need to modify the teachings thereof. Additionally, applicant submits that Subramanian does not mention difficulties with or need to improve pull-up transistors for driving I/O nodes of a semiconductor device as set forth in the claims of the present application.

Claim 5 of the present invention defines -

A pull-up transistor disposed between a Vdd terminal and an I/O pad of a semiconductor device comprising:

a semiconductor substrate of a first conductive-type;

a source region and a drain region of a second conductive type formed in the substrate and defining between them a channel region, one of the source region and the drain region being electrically coupled to the I/O pad, the other one of the source region and the drain region being electrically coupled to the Vdd terminal;

an impurity implantation region of impurities of a second conductive-type formed in a first sector of the channel region, the first sector not reaching either one of the source region and the drain region

the impurity implantation region of the first sector comprising a surface region operable under field effect as a depletion channel;

a second sector of the channel region exclusive of the first sector comprising a uniform doping concentration of the first conductive type and a surface region operable under field effect as an enhancement channel;

a gate insulating layer on the substrate over at least a portion of the surface region of the first sector and the surface region of the second sector; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector.

As noted by the Examiner in the Office Action of July 19, 2001, page 3, lines 4-6, Subramanian does not teach of a pull-up transistor between a Vdd terminal and an I/O pad. Applicant submit further that, nor does Subramanian disclose a need to modify pull-up transistors, e g., such as those of the prior art described in the present application. Accordingly it can't be said that Subramanian discloses or suggests of a pull-up transistor as defined in claim 5 of the present application.

Furthermore, claim 5 defines that a second sector of the channel region outside the first sector comprises a uniform doping concentration of the first conductive type. In contrast, Subramania (FIGS. 6-7) teaches non-uniform doping profiles (column 1, line 67 to column 2, line 1), e.g., as can be seen illustrated in the channel regions where the "*buried*

junction 24" is spaced away from the surface of the substrate beneath gate oxide layer 42. In deed, Subramanian teaches use of implant energy sufficient to form the buried junction with a dopant concentration peak beneath the surface of the substrate (column 3, lines 63-66). Accordingly, applicant submits that Subramanian teaches away from important features of the present invention as defined in claim 5.

Further, applicant submits that the Examiner, in advancing the obviousness rejection, has impermissibly combined material of the applicant's disclosure with Subramanian.

Applicant respectfully submits that the Examiner is reciting combinations and advantages per a subconscious benefit of hindsight afforded by the present patent application. Prior art references in combination do not make an invention obvious unless something in the prior art suggests a motivation for combining their teachings. It is not enough that the Examiner sites advantages; the Examiner should point to where these advantages are mentioned in the cited prior art references -- absent the present teachings of applicant.

CONCLUSION

As presented above, Subramanian, when fairly read without the benefit of the applicant's specification, does not teach or suggest the pull-up transistor of the present invention as defined in claim 5.

Accordingly, applicant submits that claim 5 is patentable over the prior art. Likewise, it follows that dependent claims 6-7 and 9 also are patentable, at least for reason of being dependent upon a patentable base claim.

In view of the above, applicant submits that claims 5-7 and 9 of the present application are allowable and respectfully request such action for this case.

The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

5. (Twice Amended) A pull-up transistor [for use with] disposed between a Vdd terminal and an I/O pad of a semiconductor device comprising:

a semiconductor substrate of a first conductive-type;

a source region and a drain region of a second conductive type formed in the substrate and defining between them a channel region, one of the source region and the drain region being electrically coupled [with] to the I/O pad, the other one of the source region and the drain region being electrically coupled [with] to the Vdd terminal;

an impurity implantation region of impurities of a second conductive-type formed in a first sector of the channel region, the first sector not reaching either one of the source region and the drain region[,];

the impurity implantation region of the first sector comprising a surface region operable under field effect as a depletion channel;

[wherein] a second sector of the channel region exclusive of the first sector [has] comprising a uniform doping concentration of the first conductive type and a surface region operable under field effect as an enhancement channel;

a gate insulating layer on the substrate over at least a portion of the surface region of the first sector and the surface region of the second sector [impurity implantation region and over at least a portion of an area adjacent the impurity implantation region]; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of [a region adjacent to the first sector] the second sector.

6. The transistor of claim 5, wherein the first sector has a narrower line width than a line width of the gate.

7. (Amended) The transistor of claim 5, [wherein] in which

the gate [is over] comprises a first portion [of] over the first sector and [over] a second portion [of an area adjacent the first] over the second sector[,]; and [wherein]

the first portion is in a predetermined ratio with respect to the second portion.

9. The transistor of claim 5, wherein the first sector is separated from the source region and from the drain region by substantially equal distances.